

REMARKS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

It has been noted that at the time of filing the utility patent application the claims were inadvertently misnumbered and filed as claims 1-67 leaving out claim 58. The Applicants respectfully request the Examiner to approve the amendments to claims 58-66.

35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1, 2, 4-20, 22-35, and 37-67 as being anticipated by U.S. Patent No. 6,088,370 (hereinafter referred to as Bell).

"To anticipate a claims, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1, 16, 29, 30, 47, and 50 of the present application includes limitations not disclosed or taught by the Bell. As a result, the independent claims 1, 16, 29, 30, 47, and 50 are not anticipated by the Bell.

In particular, the independent claims include the limitation of an interface "between a memory control *hub* (MCH) and a input/output control *hub* (ICH)".

Bell, however, does not disclose an interface between a memory control *hub* (MCH) and a input/output control *hub* (ICH). Rather, Bell only discloses a

bus system that provides “connections between a controller 115 . . . and bus expander bridges 117, 120, and 125.” (Bell Col. 2, lns. 21-27) (emphasis added).

More specifically, the examiner states that one of the bus expander bridges 117, 120, and 125 as shown in Bell disclose applicant’s claimed input/output control hub (ICH). Applicant respectfully disagrees.

The bus expander bridges 117, 120, and 125 shown and described in Bell, do not disclose applicant’s claimed input/output control hub (ICH). As defined in applicant’s detailed description, the ICH is a hub that is capable of providing an interconnection between various peripheral components and external buses, with a separate bus interface.

The expander bridges as shown in Bell are different than the input/output control hub as claimed by applicant in that the expander bridges have more limited capability. The expander bridges are unable to accept/interconnect multiple peripherals and external buses with another interface or bus. *As a result, multiple expander bridges need to be used to provide the function or service of the claimed input/output control hub.*

For example, see Figure 1 and accompanying description of Bell. As shown and described in Bell, multiple expander bridges 117, 120, and 125 are shown to interface the controller 115, compared to applicants claimed input/output control hub interfacing with the claimed MCH. The disadvantages of using the multiple expander bridges rather than the claimed input/output control hub, include the resulting increase in signal and data paths that results from having multiple expander bridges interconnected with the

controller 115, compared to the input/output control hub interface with the MCH.

For example, as shown and described in Figure 1 of Bell, there are at least 4 separate interconnections between bridges and the controller 115, **resulting in at least four different 16 bit busses/interfaces to the controller 115**. To the contrary, applicant's claimed input/output control hub results in significantly more simple interconnection than the use of the multiple bridges as shown in Bell. By way of exemplary embodiment only, as shown in applicant Figure 8 of applicant's detailed description, the interface of the input/output control hub to the MCH, includes the simple interface of only a 25 bit signal path (the actual size of an interface between an ICH and MCH may vary within the scope of the invention).

Therefore, considering the multiple expander bridges disclosed in Bell are clearly distinct and separate from the claimed input/output control hub as claimed by applicant, Bell clearly does not anticipate applicants' independent claims.

In addition, applicants' remaining claims depend from at least one of the independent claims mentioned above. As a result of depending from one of the independent claim, the remaining claims include the distinguishing limitations discussed above, and are therefore also not anticipated by Bell.

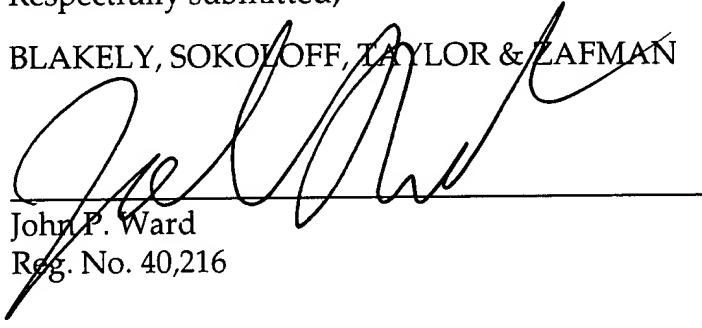
CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

  
John P. Ward  
Reg. No. 40,216

Date: 02/24/2003

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025-1026  
(408) 720-8300



ATTACHMENT A

A marked-up version of the amended claims is as follows:

1. An interface to transfer data directly between a memory control hub (MCH) and a input/ output control hub (ICH) within a computer system, comprising:
  - a data signal path to transmit data in packets via split transactions; and
  - a set of command signals, wherein said interface provides a point-to-point connection between said MCH and said ICH, exclusive of an external bus connected directly to the interface.
2. The interface of claim 1, wherein said MCH and said ICH within said computer system are components within a chipset.
3. The interface of claim 1, wherein a first transaction is initiated on said interface with a request packet, subsequent to arbitration for ownership of said interface.
4. The interface of claim 3, wherein said request packet includes a transaction descriptor.
5. The interface of claim 3, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.
6. The interface of claim 3, wherein said request packet includes transaction descriptor and said completion packet includes a corresponding transaction descriptor.

7. The interface of claim 5, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.
8. The interface of claim 3, wherein said data signal path is scalable.
9. The interface of claim 8, wherein packets are transmitted across said data signal path via a source synchronous clock mode.
10. The interface of claim 9, wherein said interface includes a set of bi-directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi-directional stop signal.
11. The interface of claim 10, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.
12. The interface of claim 11, wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.
13. The interface of claim 5, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.
14. The interface of claim 3, wherein arbitration between said hubs is symmetric and distributed.

15. The interface of claim 3, wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

16. An interface to transfer data directly between a memory control hub (MCH) and an input / output control hub (ICH) within a computer system, comprising:

    a first means for transmitting data between said MCH and said ICH in packets via split transactions; and

    a second means for transmitting command signals, wherein said interface provides a point-to-point connection between said MCH and said ICH, exclusive of an external bus connected directly to the interface.

17. The interface of claim 16, wherein said ICH and said MCH within said computer system are components within a chipset.

18. The interface of claim 17, wherein said interface includes a means for initiating a first transaction on said interface with a request packet.

19. The interface of claim 18, wherein said request packet includes a transaction descriptor.

20. The interface of claim 19, wherein said interface includes means for providing a completion packet in response to said request packet of said first transaction.

21. The interface of claim 18, wherein said request packet includes a transaction descriptor and said completion packet includes a corresponding transaction descriptor.

22. The interface of claim 21, wherein said interface includes a means for transmitting request packet for a second transaction across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.
23. The interface of claim 22, wherein said first means for transmitting data in packets via split transactions includes further includes means for scaling a data signal path.
24. The interface of claim 23, wherein said interface includes means for transmitting packets across said interface via a source synchronous clock mode.
25. The interface of claim 21, wherein said transaction descriptors include a means for identifying separate hubs within a hierarchy of multiple interfaces between three or more hubs.
26. The interface of claim 20, wherein said request packet includes a means for indicating if a completion packet is required in response to the respective request packet.
27. The interface of claim 26, wherein interface includes a means for arbitrating between said hubs for ownership of said interface.
28. The interface of claim 21, wherein said interface further includes a means for allotting ownership of said interface to one of said hubs up to a predetermined amount of time.
29. An interface to transfer data between a memory control hub and an

input/output (I/O) hub of a chipset within a computer system, comprising:

a bi-directional data signal path and a pair of source synchronous strobe signals, said data signal path transmits data in packets via split transactions, said packets including a request packet and completion packet, said request packet including a transaction descriptor; and

a set of command signals including unidirectional arbitration signal, a bi-directional stop signal, a system reset signal, a common clock signal, and a voltage reference signal, wherein said interface provides a point-to-point connection between said memory control hub and said I/O hub, exclusive of an external bus connected directly to the point-to-point connection.

30. (Amended) A computer system comprising

a processor;

a memory control hub (MCH) coupled to said processor;

an input/ output control hub (ICH) coupled to said MCH via an interface to transfer data directly between the MCH and the ICH;

said interface having a data signal path to transmit data in packets via split transactions, and said interface including a set of command signals, wherein said interface provides a point-to-[poinf]point connection between said MCH and said ICH, exclusive of an external bus connected directly to the point-to-point connection; and

at least one peripheral component coupled to said ICH.

31. The computer system of claim 30, wherein said peripheral component is a Peripheral Component Interconnect (PCI) agent.

32. The computer system of claim 31, wherein said first and second hubs within said computer system are components within a chipset.

33. The computer system of claim 32, wherein a first transaction is initiated on said interface with a request packet, subsequent to arbitration for ownership of said interface.
34. The computer system of claim 33, wherein said request packet includes a transaction descriptor.
35. The computer system of claim 33, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.
36. The computer system of claim 35, wherein said request packet includes a transaction descriptor and said completion packet includes a corresponding transaction descriptor.
37. The computer system of claim 36, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.
38. The computer system of claim 36, wherein said data signal path is scalable.
39. The computer system of claim 38, wherein packets are transmitted across said data signal path via a source synchronous clock mode.
40. The computer system of claim 39, wherein said interface includes a set of bi-directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi-directional stop signal.

41. The computer system of claim 40, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.

42. The computer system of claim 41, wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.

43. The computer system of claim 42, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

44. The computer system of claim 43, wherein arbitration between said hubs is symmetric and distributed.

45. The computer system of claim 44, wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

46. The computer system of claim 31, wherein the computer system includes multiple processors.

47. The computer system of claim 31, wherein the computer system further includes a third hub coupled to said ICH via an interface comprising:

    a bi-directional data signal path and a pair of source synchronous strobe signals, said data signal path transmits data in packets via split transactions, said packets including a request packet and completion packet, said request packet including a transaction descriptor; and

a set of command signals including unidirectional arbitration signal, a bi-directional stop signal, a system reset signal, a common clock signal, and a voltage reference signal.

48. The computer system of claim 31, wherein the processor and the MCH of said computer system, are integrated on a single semiconductor unit.

49. The computer system of claim 31, wherein the MCH and a graphics unit of said computer system, are integrated on a single semiconductor unit.

50. A memory control hub (MCH) comprising:

an interface to transfer data directly to an input/ output control hub (ICH) within a computer system, the interface having a data signal path to transmit data in packets via split transactions, and a set of command signals, wherein the interface provides a point-to-point connection between said the MCH and said ICH, exclusive of an external bus connected directly to the interface.

51. The memory control hub of claim 50, wherein said MCH and ICH are components within a chipset.

52. The memory control hub of claim 50, wherein a first transaction is initiated on said interface with a request packet, subsequent to arbitration for ownership of said interface.

53. The memory control hub of claim 52, wherein said request packet includes a transaction descriptor.

54. The memory control hub of claim 53, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.

55. The memory control hub of claim 52, wherein said request packet includes transaction descriptor and said completion packet includes a corresponding transaction descriptor.

56. The memory control hub of claim 55, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.

57. The memory control hub of claim 56, wherein said data signal path is scalable.

58<sup>[59]</sup>.(Amended)The memory control hub of claim 57, wherein packets are transmitted across said data signal path via a source synchronous clock mode.

59<sup>[60]</sup>.(Amended) The memory control hub of claim 58<sup>[59]</sup>, wherein said interface includes a set of bi- directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi- directional stop signal.

60<sup>[61]</sup>.(Amended) The memory control hub of claim 59<sup>[60]</sup>, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.

61[62]. (Amended) The memory control hub of claim 60[61], wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.

62[63]. (Amended) The memory control hub of claim 61[62], wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

63[64]. (Amended) The memory control hub of claim 62[63], wherein arbitration between said hubs is symmetric and distributed.

64[65]. (Amended) The memory control hub of claim 63[64], wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

65[66]. (Amended) The memory control hub of claim 50, wherein the memory control hub and a processor are integrated on a single semiconductor unit.

66[67]. (Amended) The memory control hub of claim 50, wherein the memory control hub and a graphics unit are integrated on a single semiconductor unit.